UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,406	07/16/2003	Kelvin S. Vartti	RA-5623	1541

7590 12/31/2007

Beth L. McMahon
Unisys Corporation
MS 4773
P.O. Box 64942
St. Paul, MN 55164

EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

MAIL DATE	DELIVERY MODE
12/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,406	VARTTI ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *2,4,17,18 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-16,19-28 and 30-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The indicated allowability of claim 4 is withdrawn in view of the newly discovered reference(s) to US 5,644,753 (Ebrahim et al). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 5-16, 19-28, and 30-37 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,644,753 (Ebrahim et al).

With respect to claim 1, Ebrahim discloses the invention as claimed, a memory system, comprising: a programmable storage device to store one or more indicators [(Etag and Dtag, Fig. 1 and 12 for storing line identifier) Col. 4, Lines 1-5; Col. 13, Lines 37-66]; a cache [cache 440, Fig. 12]; a requester to request data from, and store data to the cache [cache access request to cache memory 400 is initiated by data processor 402, each data processor including master interface for sending memory transaction requests to system controller and receiving cache access requests from the controllers) Col. 4, Lines 6-13]; a main memory to provide requested data that is not stored within the cache [(a main memory (108, Fig. 1) coupled to a system controller to service

requests missing the cache) Col. 3, Lines 14-32]; cache tag logic [cache tag array 406, Fig. 12]; a control circuit coupled to the requester, the storage device, the cache, and to the cache tag logic [cache logic 444, Fig. 12], the control circuit to receive data and to determine, based on the state of the one or more indicators, whether to update the cache tag logic to track the data [(control logic including comparator to process address values and generate hit/miss signals) Col. 4, Lines 21-30], and based on the state of the one or more indicators, to determine whether to store the data in the cache, and if so, to replace the received data in the cache [state value stored in the corresponding cache tag 412 will be updated if necessary to indicate that modified data is stored in the cache line) Col. 3, Line 11-40] .

With respect to claim 3, Ebrahim teaches the invention wherein one of the indicators indicates the cache is not available for use [(multiple modes including write back mode and including early indication of dirty data restricting outstanding dirty victim writeback transactions or restriction of requests associated with exclusive modified state or an invalidation operation) Col. 28, Lines 28-52; Col. 27, Lines 8-52].

With respect to claim 5, Ebrahim teaches the invention wherein the main memory provides data to the cache in response to a request that is any one of multiple request types, wherein at least one of the indicators identifies one or more of the request types, and wherein the control circuit prevents the replacement of the data in the cache if the data was provided in response to any of the identified request types [(multiple modes

including write back mode and including early indication of dirty data restricting outstanding dirty victim writeback transactions or restriction of requests associated with exclusive modified state or an invalidation operation) Col. 28, Lines 28-52; Col. 27, Lines 8-52].

With respect to claim 6, Ebrahim teaches the invention wherein the one or more request types includes a request type indicating the data will be modified by a requester [(multiple modes including write back mode and including early indication of dirty data restricting outstanding dirty victim writeback transactions or restriction of requests associated with exclusive modified state or an invalidation operation) Col. 28, Lines 28-52; Col. 27, Lines 8-52].

With respect to claim 7, Ebrahim teaches the invention wherein at least one of the indicators identifies one or more of the at least one requester, and wherein the control circuit replaces the data in the cache if the data was returned from the main memory in response to a request Issued by any of the identified requesters [regular copyback at the conclusion of the transaction) Col. 27, Lines 33-45].

With respect to claim 8, Ebrahim teaches the invention wherein the main memory provides data to the cache with a response that is any one of multiple response types, wherein at least one of the indicators Identifies one or more of the response types, and wherein the control circuit replaces the data in the cache if the data is returned from the main memory with any of the identified response types [(multiple modes including write back mode and including early indication of dirty data restricting outstanding dirty victim

writeback transactions or restriction of requests associated with exclusive modified state or an invalidation operation) Col. 28, Lines 28-52; Col. 27, Lines 8-52].

With respect to claims 9-16, 19-28, and 30-37, please refer to the analysis of claim rejection, as addressed above with respect to claims 1, 3, and 5-8.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 7,181,572 (Walmsley) teaches cache method and apparatus including cache, a processor, a memory interface wherein following a cache miss, using the processor to issue a request, using the memory interface to fetch the first data from main memory, and sending the first data to the processor; updating the cache with the first data and (e) updating flags in the cache associated with the first data.

US 6,647,469 (Sharma et al) teaches using read current transactions for improved performance in directory-based coherent I/O systems wherein an I/O device makes a read request, which is sent to I/O bus interface and then sent to the cache unit and wherein the I/O device's request asks the cache unit to provide the data ad the cache unit cache controller looks to the cache tag to determine if that specific cache line is in use.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon, Tue-Fri (8:00A to 5:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186